CLAIMS

1. (Currently amended) Apparatus, comprising an asymmetry-changing circuit adapted to (i) process a first signal having positive and negative pulses and characterized by a first asymmetry and (ii) based on the first signal, generate a second signal having positive and negative pulses and characterized by a second asymmetry different from the first asymmetry, wherein:

the second signal is generated by providing a signal contribution corresponding to a higher-than-second order of the first signal;

the first signal has positive and negative pulses of different amplitudes;

the second signal has positive and negative pulses of substantially uniform amplitudes;

the asymmetry-changing circuit comprises an asymmetry-reducing circuit adapted to process the first signal and, based on the first signal, generate the second signal, wherein the second signal is generated by providing a signal contribution corresponding to a third order of the first signal; and

the asymmetry-reducing circuit comprises:

a differential amplifier having two differential inputs and two differential outputs, wherein the second signal appears at the differential outputs; and

a plurality of MOS devices connected to the differential inputs and outputs such that conductance of the MOS devices provides input and feedback resistances to the differential amplifier.

2. (Canceled)

3. (Currently amended) The apparatus of claim 1 [[2]], wherein the second signal is generated by providing at least one of:

an additional signal contribution corresponding to a second order of the first signal; and

further signal contributions corresponding to orders of the first signal higher than the third order.

4-7. (Canceled)

8. (Currently amended) The apparatus of claim 1 [[7]], wherein the asymmetry-reducing circuit further comprises a switch set adapted to couple the MOS devices to the first signal to modulate the conductance of the MOS devices with the first signal such that the input and feedback resistances are modulated in a complementary manner.

9. (Original) The apparatus of claim 8, wherein:

each MOS device comprises an arrayed MOS transistor having a source, a drain, and a plurality of fingers adapted to control source-to-drain conductance of said transistor, said source-to-drain conductance determining the conductance of the MOS device; and

the switch set is adapted to couple the fingers to the first signal such that, for each MOS device, the coupling of any two fingers is independent of each other.

10. (Original) The apparatus of claim 9, wherein the switch set has at least one switch adapted to couple a corresponding finger to a signal selected from positive and negative copies of the first signal.

11. (Original) The apparatus of claim 9, wherein the switch set has at least one switch adapted to couple a corresponding finger to a signal corresponding to a fraction of a difference between positive and negative copies of the first signal.

12. (Original) The apparatus of claim 8, wherein the switch set is controlled by a control signal generated based on the amplitude differences in the first signal.

13. (Original) The apparatus of claim 7, wherein the plurality of MOS devices comprises first, second, third, and fourth MOS devices, wherein:

the first and second MOS devices provide the feedback resistances; and

the third and fourth MOS devices provide the input resistances.

14. (Original) The apparatus of claim 13, wherein:

each MOS device has a source and a drain; and

for the first MOS device:

the source is adapted to receive a signal corresponding to a positive copy of the first signal; and

the drain is connected to a first differential input;

for the second MOS device:

the source is adapted to receive a signal corresponding to a negative copy of the first signal; and

the drain is connected to a second differential input;

for the third MOS device:

the source is coupled to a first differential output; and

the drain is connected to the first differential input and the drain of the first MOS device; and

for the fourth MOS device:

the source is coupled to a second differential output; and

the drain is connected to the second differential input and the drain of the second MOS device.

15. (Original) The apparatus of claim 14, wherein:

the signal received by the source of the first MOS device is generated by a first source follower;

the signal received by the source of the second MOS device is generated by a second source follower;

the source of the third MOS device is coupled to the first differential output via a third source follower; and

the source of the fourth MOS device is coupled to the second differential output via a fourth source follower.

16. (Currently amended) The apparatus of claim 1 [[2]], wherein:

the first signal corresponds to a signal generated by a read head of a magnetic disk drive; and

the asymmetry-reducing circuit is implemented in an integrated circuit and is a part of read/write channel of the magnetic disk drive.

17. (Currently amended) A method of reducing signal asymmetry, comprising:

(A) receiving a first signal having positive and negative pulses of different amplitudes; and

(B) based on the first signal, generating a second signal having positive and negative pulses of substantially uniform amplitudes, wherein:

the second signal is generated by providing a signal contribution corresponding to a greater-than-second order of the first signal; and

step (B) comprises modulating a gain of a variable-gain amplifier by the first signal, wherein the variable-gain amplifier is adapted to implement substantially the following transfer function:

$$y(t) = z(t)\exp(-cz(t)),$$

where $z(t)$ denotes the first signal, $y(t)$ denotes the second signal, and c is a constant corresponding to the amplitude differences in the first signal.

18. (Original) The method of claim 17, wherein, in step (B), the second signal is generated by providing a signal contribution corresponding to a third order of the first signal.

19-20. (Canceled)

21. (New) Apparatus, comprising an asymmetry-changing circuit adapted to (i) process a first signal having positive and negative pulses and characterized by a first asymmetry and (ii) based on the first signal, generate a second signal having positive and negative pulses and characterized by a second asymmetry different from the first asymmetry, wherein:

the second signal is generated by providing a signal contribution corresponding to a higher-than-second order of the first signal;

the first signal has positive and negative pulses of different amplitudes;

the second signal has positive and negative pulses of substantially uniform amplitudes;

the asymmetry-changing circuit comprises an asymmetry-reducing circuit adapted to process the first signal and, based on the first signal, generate the second signal, wherein the second signal is generated by providing a signal contribution corresponding to a third order of the first signal; and

the asymmetry reducing circuit comprises two serially connected circuits, wherein each of the serially connected circuits is adapted to generate an output signal corresponding to a second-order function of a signal applied to said serially connected circuit.

22. (New) The apparatus of claim 21, wherein:

each of the serially connected circuits comprises two signal paths coupled to a summation circuit adapted to generate the output signal by adding signals received via the two paths; and

one of the signal paths comprises (I) a square-term generator adapted to square an applied signal and (II) a linear multiplier adapted to multiply a signal produced by the square-term generator by a constant.

23. (New) Apparatus, comprising an asymmetry-changing circuit adapted to (i) process a first signal having positive and negative pulses and characterized by a first asymmetry and (ii) based on the first signal, generate a second signal having positive and negative pulses and characterized by a second asymmetry different from the first asymmetry, wherein:

the second signal is generated by providing a signal contribution corresponding to a higher-than-second order of the first signal;

the first signal has positive and negative pulses of different amplitudes;

the second signal has positive and negative pulses of substantially uniform amplitudes;

the asymmetry-changing circuit comprises an asymmetry-reducing circuit adapted to process the first signal and, based on the first signal, generate the second signal, wherein the second signal is generated by providing a signal contribution corresponding to a third order of the first signal; and

the asymmetry-reducing circuit comprises two signal paths coupled to a multiplier circuit adapted to generate the second signal by multiplying signals received via the two paths, wherein one of the signal paths comprises (I) a linear multiplier adapted to multiply the first signal by a constant and (II) an exponential-term generator adapted to generate an output signal having an amplitude substantially equal to the exponent of a signal produced by the linear multiplier.

24. (New) A method of reducing signal asymmetry, comprising:

(A) receiving a first signal having positive and negative pulses of different amplitudes; and

(B) based on the first signal, generating a second signal having positive and negative pulses of substantially uniform amplitudes, wherein:

the second signal is generated by providing a signal contribution corresponding to a greater-than-second order of the first signal; and

step (B) comprises modulating a gain of a variable-gain amplifier by the first signal, wherein the variable-gain amplifier is adapted to implement substantially the following transfer function:

$$y(t) = z(t)\frac{1-\frac{c}{2}z(t)}{1+\frac{c}{2}z(t)},$$

where *z(t)* denotes the first signal, *y(t)* denotes the second signal, and *c* is a constant corresponding to the amplitude differences in the first signal.